EiceDRIVER(tm)

High voltage gate driver IC

2EDL family

600 V half bridge gate drive IC
2EDL05I06PF
2EDL05I06PJ
2EDL05I06BF
2EDL05N06PF
2EDL05N06PJ
2EDL23I06PJ
2EDL23N06PJ

EiceDRIVER(TM)

Target datasheet

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Page or Item	**Subjects (major changes since previous revision)**
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p. 9	Revised Figure 2
pp.17	Introduced Iopk+ and Iopk- values
all	introduced 2EDL05N06PJ

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EiceDRIVER(tm)
600 V half bridge gate drive IC

PG-DSO-8

PG-DSO-14

1 Overview

Main features

- Thin-film-SOI-technology
- Maximum blocking voltage +600V
- Individual control circuits for both outputs
- Filtered detection of under voltage supply
- All inputs clamped by diodes
- Off line gate clamping function
- Asymmetric undervoltage lockout thresholds for high side and low side
- Qualified according to JEDEC[1] (high temperature stress tests for 1000h) for target applications

Product highlights

- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Ultra fast bootstrap diode
- Overcurrent comparator (2EDL23I06PJ and 2EDL23N06PJ only)
- Enable function, Fault indicator (2EDL23I06PJ and 2EDL23N06PJ only)

Typical applications

- Home appliances
- Consumer electronics
- Fans, pumps
- General purpose drives

Product family

Table 1 Members of 2EDL family

Sales Name	Special function	output current	Target transistor	typ. LS UVLO-thresholds	Bootstrap diode	Package
2EDL05I06PF 2EDL05I06PJ	deadtime, interlock	0.5 A	IGBT	12.5 V / 11.6 V	Yes	DSO-8 DSO-14
2EDL05I06BF	–	0.5 A	IGBT	12.5 V / 11.6 V	Yes	DSO-8
2EDL05N06PF 2EDL05N06PJ	deadtime, interlock	0.5 A	MOSFET	9 V / 8.1 V	Yes	DSO-8 DSO-14
2EDL23I06PJ	deadtime, interlock, Enable, Fault, OCP	2.3 A	IGBT	12.5 V / 11.5 V	Yes	DSO-14
2EDL23N06PJ	deadtime, interlock, Enable, Fault, OCP	2.3 A	MOSFET	9 V / 8.1 V	Yes	DSO-14

[1] J-STD-020 and JESD-022

Description

The 2EDL family contains devices, which control power devices like MOS-transistors or IGBTs with a maximum blocking voltage of +600V in half bridge configurations. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions.

The two independent drivers outputs are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic which are optimised either for IGBT or MOSFET.

Those parts, which are designed for IGBT have asymmetric undervoltage lockout levels, which support strongly the integrated ultrafast bootstrap diode. Additionally, the offline gate clamping function provides an inherent protection of the transistors for parasitic turn-on by floating gate conditions, when the IC is not supplied via VCC.

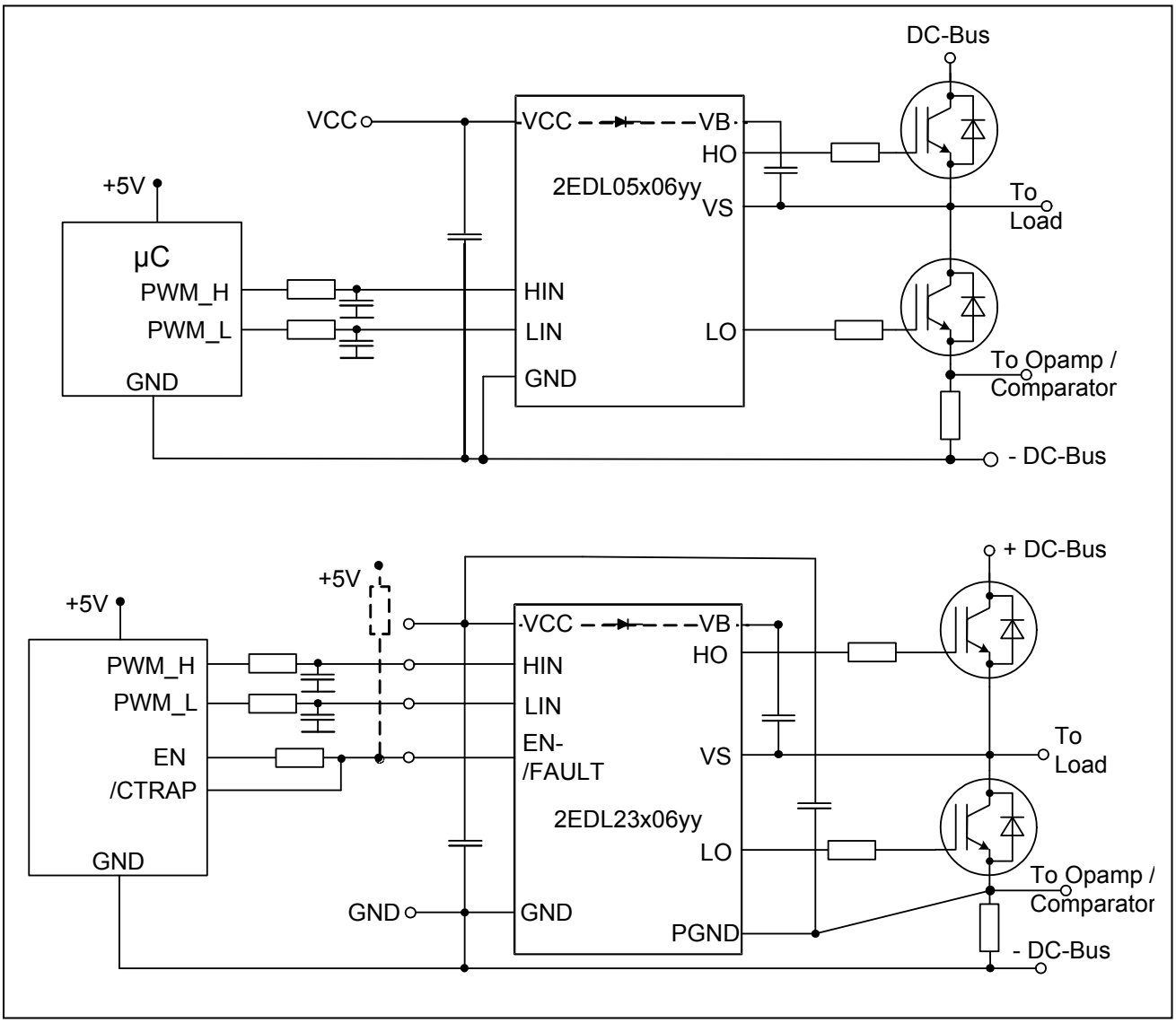

Figure 1 Typical Application (Top: SO8 / SO14 package; Bottom: SO14 package)

2 Blockdiagram

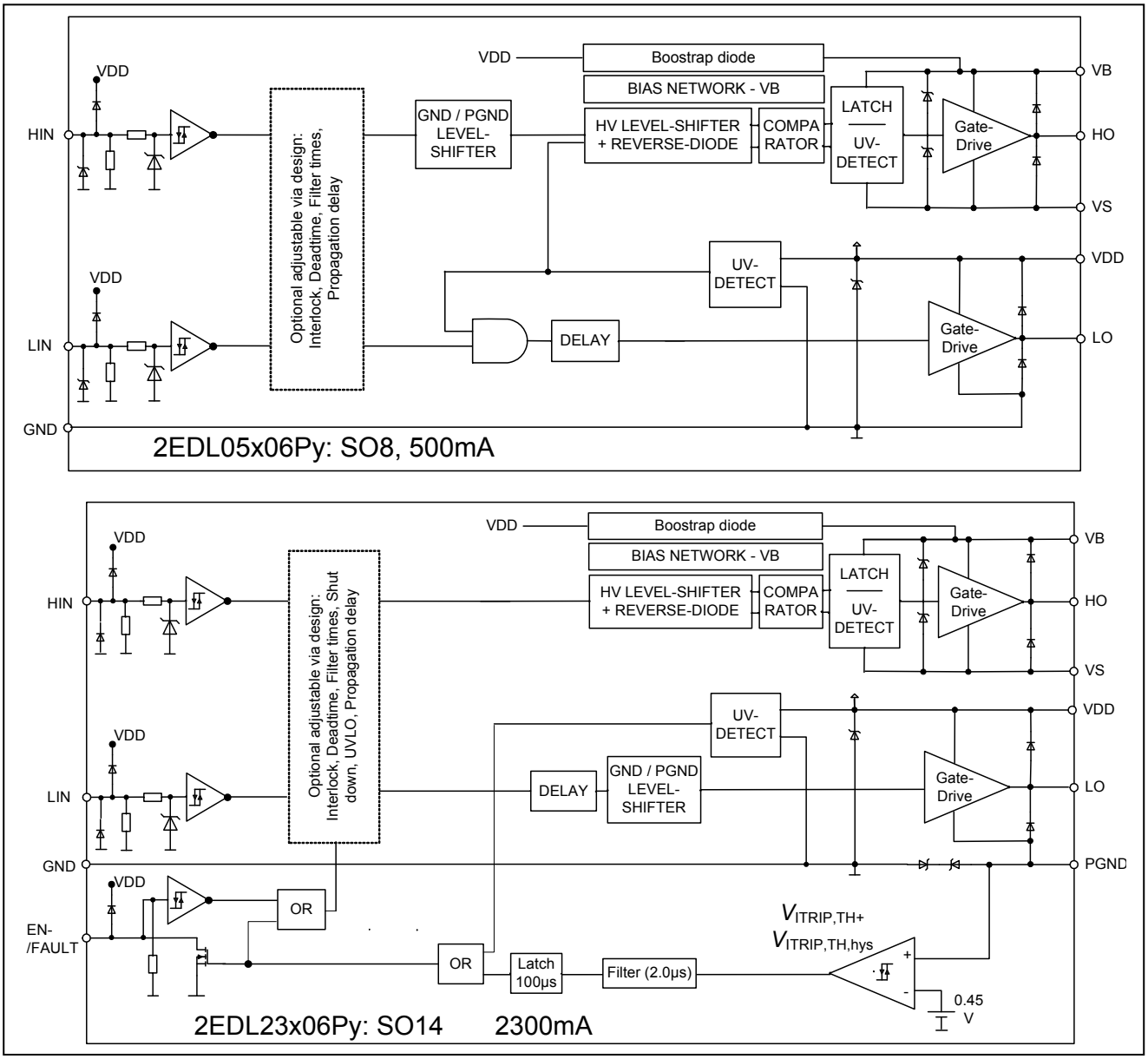

Figure 2 Block diagram for 2EDL05x06Py, 2EDL23x06Py

3 Pin configuration, description, and functionality

3.1 Pin Configuration and Description

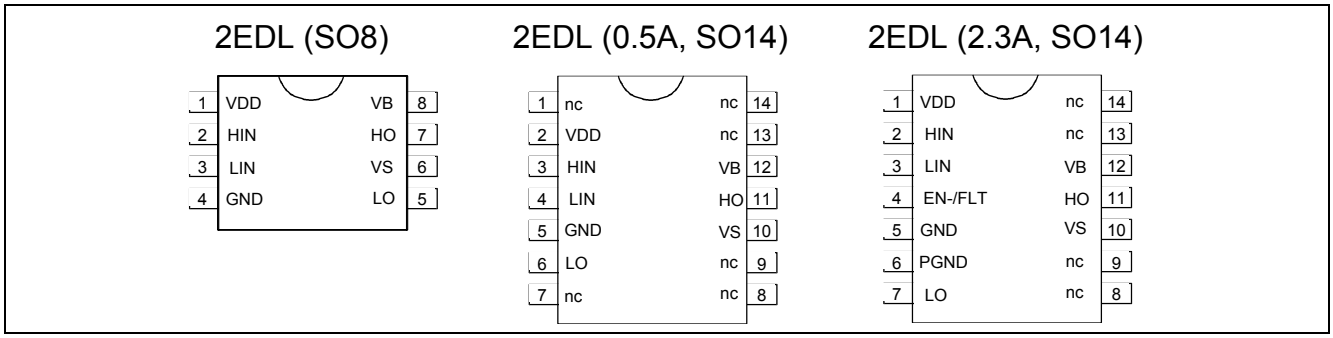

Figure 3 Pin Configuration of 2EDL family

Table 2 Pin Description

Symbol	Description
VCC	Low side power supply
GND	Logic ground
HIN	High side logic input
LIN	Low side logic input
PGND	Low side gate driver reference
VB	High side positive power supply
HO	High side gate driver output
VS	High side negative power supply
LO	Low side gate driver output
nc	Not Connected

3.2 Low Side and High Side Control Pins (LIN, HIN)

3.2.1 Input voltage range

All input pins have the capability to process input voltages up to the supply voltage of the IC. The inputs are therefore internally clamped to VCC and GND by diodes. An internal pull-down resistor is high ohmic, so that it can keep the IC in a safe state in case of PCB crack.

3.2.2 Switching levels

The Schmitt trigger input threshold is such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. The input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4 and Figure 5. Please note, that the switching levels of the input structures remain constant even though they can accept amplitudes up to the IC supply level.

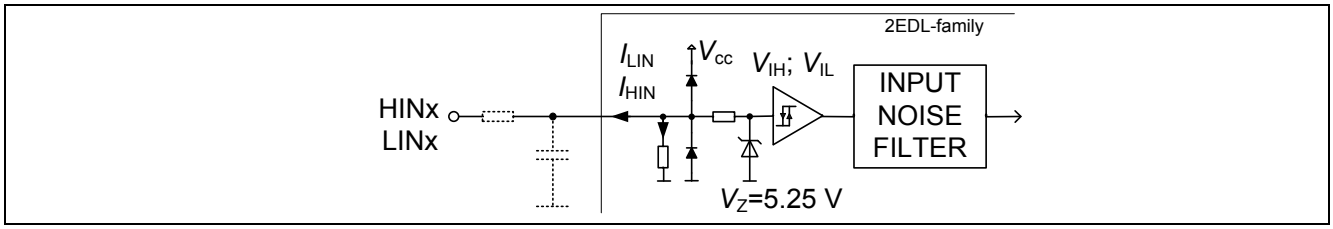

Figure 4 Input pin structure

3.2.3 Input filter time

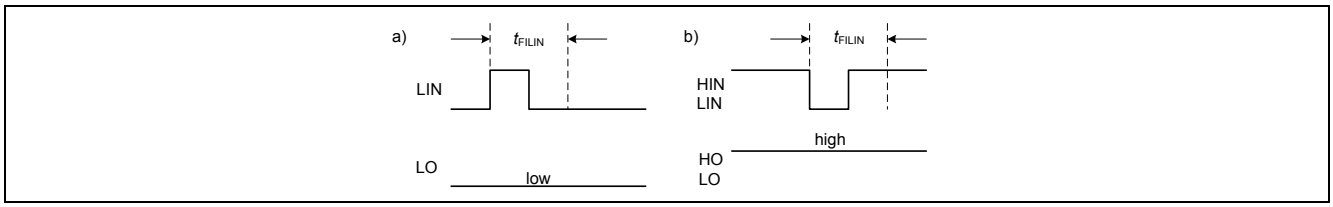

Figure 5 Input filter timing diagram

Short pulses are suppressed by means of an input filter. All IC, which have undervoltage lockout (UVLO) thresholds for MOSFET, have an input filter time of t_{FILIN} = 75 ns typ. and 150ns max. All IC having UVLO thresholds for IGBT have filter times of t_{FILIN} = 150 ns min and 200ns typ.

3.3 VCC, GND and PGND (Low Side Supply)

VCC is the low side supply and it provides power to both the input logic and the low side output power stage. The input logic is referenced to GND ground as well as the under-voltage detection circuit. Output power stage is referenced to PGND ground. PGND ground is floating respect to GND ground with a absolute maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The undervoltage lockout circuit enables the device to operate at power on when a typical supply voltage higher than V_{CCUV+} is present. Please see section 3.6 “Undervoltage lockout”” for further information.

A filter time of typ. 2 µs helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

3.4 VB and VS (High Side Supplies)

VB to VS is the high side supply voltage. The high side circuit can float with respect to GND following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VCC. A filter time of typ. 1.3 µs helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than V_{CCUV+} is present. Please see section 3.6 “Undervoltage lockout” for further information. Details on bootstrap supply section and transient immunity can be found in application note AN-Gatedrive-6ED2-1.

3.5 LO and HO (Low and High Side Outputs)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive for IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs. In particular, after an undervoltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the high side output. In contrast, the low side outputs switch to the state of their respective inputs after a undervoltage condition of the VCC supply.

The output current specification I_{O+} and I_{O-} is defined in a way, which considers the power transistors miller voltage.This helps to design the gate drive better in terms of the application needs. Nevertheless, the devices are also characterised for the value of the pulse short circuit value I_{Opk+} and $I_{Opk–}$.

3.6 Undervoltage lockout (UVLO)

Two different UVLO options are required for IGBT and MOSFET. The types 2EDL05I06Px and 2EDL23I06Px are designed to drive IGBT. There are higher levels of undervoltage lockout for the low side UVLO than for the high side. This supports an improved start up of the IC, when bootstrapping is used. The thresholds for the low side are typically V_{CCUV+} = 12.5 V (positive going) and V_{CCUV-} = 11.6 V (negative going). The thresholds for the high side are typically V_{BSUV+} = 11.6 V (positive going) and V_{BSUV-} = 10.7 V (negative going).

The types 2EDL05N06Px and 2EDL23N06Px are designed to drive power MOSFET. A similar distinction for the high side and low side UVLO threshold as for IGBT is not realised here. The IC shuts down all the gate drivers power outputs, when the supply voltage is below typ. V_{CCUV-} = 8.1 V (min. / max. = 7.5V / 8.8V). The turn-on threshold is typ. V_{CCUV+} = 9 V (min. / max. = 8.3 V / 9.8 V)

3.7 Bootstrap diode

An ultra fast bootstrap diode is monolithically integrated for establishing the high side supply. Thedifferential resistor of the diode helps to avoid extremely high inrush currents when charging the bootstrap capacitor initially.

3.8 Deadtime and interlock function

The IC provides an hardware fixed deadtime. The deadtime is different for the two MOSFET types (2EDL05N06Px and 2EDL23N06Px) and for the three IGBT types (2EDL05I06Px and 2EDL23I06Px). The deadtimes are particularly typ. 400 ns for IGBT and typ. 75 ns for MOSFET. An additional interlock function prevents the two outputs from being activated simultaneously.

The part 2EDL05I06BF does not have the deadtime feature and also not the interlock function. Here, the two outpus can be activated simultaneously.

3.9 EN-/FLT (fault indication and enable function, 2EDL23x06Py only)

The types 2EDL23x06Py provide a pin, which can either be used to shut down the IC or to read out a failure status of the IC. The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. An integrated pull down resistor shuts down the IC in case of a floating input. The internal structure of the pin is given in Figure 6. The switching levels of the Schmitt-Trigger are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 0.9 V. The typical propagation delay time is t_{EN} = 500 ns. The input is clamped by diodes to VCC and GND. The input voltage range are the same as the input control pins with a max. of 20 V.

The /FLT function is an active low open-drain output indicating the status of the gate driver (see Figure 6). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details). The fault signal is activate as long as UVLO is given during power up.
- Overcurrent detection (ITRIP): The fault condition is latched until the overcurrent trigger condition is finished and additional typ. 200 µs are elapsed.

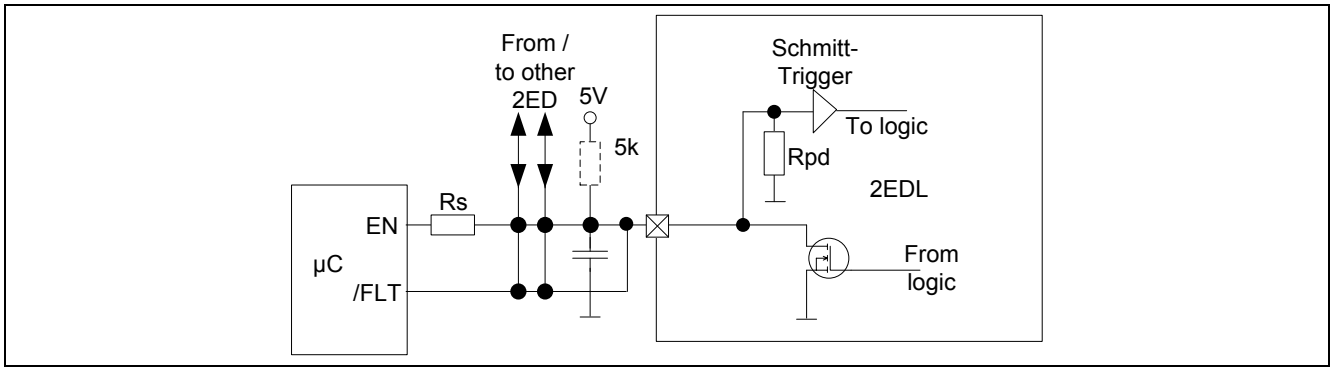

Figure 6 EN-/FLT pin structures

Power ground / over current protection (2EDL23x06Py only)

A power ground (PGND) connects directly the emitter or source of the low side transistor with the gate drive IC. No other components, such as shunts, etc., are between this connection and the emitter or source. This enables the routing of smallest gate circuit loops and therefore smallest gate inductances.

A potential shunt resistor is between the power ground (PGND) connection and the gound connection (GND), which leads to a voltage drop between these two pins.

The voltage drop between PGND and GND can be seen sensed by means of a comparator with a threshold of $V_{th,ITRIP}$ = 0.45 V. If the voltage drop is larger than $V_{th,ITRIP}$, then the output of the comparator is triggered and the /FLT output is activated. Simultaneously, the IC shuts down both gate outputs for the period of the fault indication, which is 200 µs.

Several influences, such as reverse recovery currents, parasitic inductances and other noise sources, make the need of a signal filter necessary. The filter has a time constant of typically 2.0 µs to ensure good noise quality.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a=25°C)

Table 3 Abs. maximum ratings

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage(Note 1)		V_S	V_{CC}-V_{BS}-6	600	V
High side offset voltage (t_p<500ns, Note 1)			V_{CC} -V_{BS} – 50	–	
High side offset voltage(Note 1)		V_B	V_{CC} – 6	620	
High side offset voltage (t_p<500ns, Note 1)			V_{CC} – 50	–	
High side floating supply voltage (V_B vs. V_S) (internally clamped)		V_{BS}	-1	20	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)		V_{CC}	-1	20	
Low side supply voltage (V_{CC} vs. V_{PGND})		V_{CCPGND}	-0.5	25	
Gate driver ground		V_{PGND}	-5.7	5.7	
Low side output voltage (V_{LO} vs. V_{PGND})		V_{LO}	-0.5	V_{CCPGND} + 0.5	
Input voltage LIN,HIN,EN		V_{IN}	-0.5	V_{CC} + 0.5	
FAULT output voltage		V_{FLT}	-0.5	V_{CC} + 0.5	
Power dissipation (to package) Note 2	DSO8 DSO14	P_D	– –	tbd tbd	W
Thermal resistance (junction to ambient, see section 6)	DSO8 DSO14	$R_{th(j-a)}$	– –	tbd tbd	K/W
Junction temperature		T_J	–	tbd	°C
Storage temperature		T_S	- 40	150	
offset voltage slew rate		dV_S/dt	–	50	V/ns

Note :The minimum value for ESD immunity is 1.0kV (Human Body Model) for 0.5A type and 2kV for 2.3A types. ESD immunity inside pins connected to the low side (VCC, HIN, LIN, FAULT, EN, GND, PGND, LOx) and pins connected inside each high side itself (VB, HO, VS) is guaranteed up to 1.5kV (Human Body Model) and 2kV respectively.

Note 1 : In case V_{CC} > V_B there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx in case of activated bootstrap diode. Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization.

Note 2: Consistent power dissipation of all outputs. All parameters inside operating range.

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a = 25°C)

Table 4 Required Operation Conditions

Parameter	Symbol	Min.	Max.	Unit
High side offset voltage (Note 1)	V_B	7	620	V
Low side supply voltage (V_{CC} vs. V_{PGND})	V_{CCPGND}	10	25	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a = 25°C)

Table 5 Operating range

Parameter		Symbol	Min.	Max.	Unit
High side floating supply offset voltage		V_S	V_{CC} - V_{BS} -1	500	V
High side floating supply offset voltage (V_B vs. V_{CC}, statically)		V_{BCC}	-1.0	500	
High side floating supply voltage (V_B vs. V_S, Note 1)	IGBT-Types	V_{BS}	13	17.5	
	MOSFET-Types		10	17.5	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	10	V_{BS}	
Low side output voltage (V_{LO} vs. V_{PGND})		V_{LO}	0	V_{CC}	
Low side supply voltage	IGBT-Types	V_{CC}	13	17.5	
	MOSFET-Types		10	17.5	
Low side ground voltage		V_{PGND}	-2.5	2.5	
Logic input voltages LIN,HIN,EN (Note 2)		V_{IN}	0	17.5	
FAULT output voltage	2EDL23x06Py	V_{FLT}	0	V_{CC}	
Pulse width for ON or OFF (Note 3)	IGBT-Types	t_{IN}	0.8	–	µs
	MOSFET-Types		0.3	–	
Ambient temperature		T_a	-40	95	°C
Junction temperature		T_J	tbd	125	

Note 1 : Logic operational for V_B (V_B vs. V_{GND}) > 7.0V

Note 2 : All input pins (HIN, LIN) and EN pin are internally clamped (see abs. maximum ratings)

Note 3 : The input pulse may not be transmitted properly in case of input pulse width at LIN and HIN below 0.8µs (IGBT types) or 0.3 µs (MOSFET) respectively

4.4 Static logic function table

VCC	VBS	ENABLE*	FAULT*	PGND*	LO1,2,3	HO1,2,3
<V_{CCUV-}	X	X	0	X	0	0
15V	<V_{BSUV-}	3.3 V	High imp.	< $V_{th,ITRIP}$	LIN	0
15V	15V	3.3 V	0	> $V_{th,ITRIP}$	0	0
15V	15V	0 V	High imp.	X	0	0
15V	15V	3.3 V	High imp.	< $V_{th,ITRIP}$	LIN	HIN

*) only for types 2EDL23x06Py; all voltages with reference to GND

4.5 Static parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. (T_a = 25°C) and V_{GND} = V_{PGND} unless otherwise specified

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
EN positive going threshold		$V_{EN,TH+}$	1.7	2.1	2.4		
EN negative going threshold		$V_{EN,TH-}$	0.7	0.9	1.1		
High level output voltage 0.5A types 0.5A types	LO HO	V_{OH}	– –	V_{CC} -0.7 V_B -0.7	V_{CC} -1.4 V_B -1.4		I_O = - 20 mA
High level output voltage 2.3A types	LO HO	V_{OH}	– –	V_{CC} -0.7 V_B -0.7	V_{CC} -1.4 V_B -1.4		I_O = - 100 mA
Low level output voltage 0.5A types	LO HO	V_{OL}	– –	V_{GND}+ 0.2 V_S+ 0.2	V_{GND}+ 0.6 V_S + 0.6		I_O = 20 mA
High level output voltage 2.3A types	LO HO	V_{OL}	– –	V_{PGND} +0.7 V_S +0.7	V_{PGND} - 1.4 V_S +1.4		I_O = 100 mA
V_{CC} supply undervoltage positive going threshold	IGBT-types	V_{CCUV+}	11.8	12.5	13.2		
	MOSFET types		8.3	9	9.8		
V_{BS} supply undervoltage positive going threshold	IGBT-types	V_{BSUV+}	10.9	11.6	12.4		
	MOSFET types		8.3	9	9.8		
V_{CC} supply undervoltage negative going threshold	IGBT-types	V_{CCUV-}	10.9	11.6	12.4		
	MOSFET types		7.5	8.1	8.8		
V_{BS} supply undervoltage negative going threshold	IGBT-types	V_{BSUV-}	10	10.7	11.7		
	MOSFET types		7.5	8.1	8.8		
V_{CC} and V_{BS} supply UVLO hysteresis	IGBT-types	V_{CCUVH}	0.5	0.9	–		
	MOSFET types	V_{BSUVH}	0.5	0.9	–		
ITRIP comparator threshold		$V_{th,ITRIP}$	0.38	0.44	0.51		V_{ITRIP} = V_{PGND} - V_{GND}
ITRIP comparator hysteresis		$V_{th,ITRIP\ hys}$	0.045	0.07	–		

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Offline gate clamping voltage	0.5A types	V_{CLAMP}	–	tbd	–	V	I_{O-} = tbd
	2.3A types						I_{O-} = tbd
High side leakage current betw. VS and GND		I_{LVS+}	–	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and GND		I_{LVS+}[1]	–	10	–		T_J = 125 °C, V_S = 600 V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	–	150	300		HO = low depending on current types
Quiescent current V_{BS} supply (VB only)		I_{QBS2}	–	150	300		HO = high depending on current types
Quiescent current VCC supply (VCC only)		I_{QCC1}	–	0.5	1	mA	V_{LIN} = float. V_{VSx} = 50V
Quiescent current VCC supply (VCC only)		I_{QCC2}	–	0.5	1		V_{LIN} = 3.3 V, V_{HIN}=0 V_{VSx} = 50V
Quiescent current VCC supply (VCC only)		I_{QCC3}	–	0.5	1		V_{LIN}=0 , V_{HIN}=3.3 V V_{VSx}=50V
Input bias current		I_{LIN+}	20	35	50	µA	V_{LIN} = 3.3 V
Input bias current		I_{LIN-}	–	0	–		V_{LIN} = 0
Input bias current		I_{HIN+}	20	35	50		V_{HIN} = 3.3 V
Input bias current		I_{HIN-}	–	0	–		V_{HIN} = 0
Input bias current (EN=high)		I_{EN+}	–	35	50		V_{ENABLE} = 3.3 V
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	0.5 A types	I_{O+}	0.19	0.25	–	A	C_L = 10 nF
	2.3 A types[1]		1.3	1.8	–		C_L = 47 nF
Peak output current turn on (single pulse)	0.5 A types	I_{Opk+}[1]	–	0.37	–		R_L = 0 Ω, t_p <10 µs
	2.3 A types		–	tbd	–		
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	0.5 A types	I_{O-}	0.4/tbd	0.50	–		C_L = 10 nF
	2.3 A types[1]		1.65	2.3	–		C_L = 47 nF
Peak output current turn off (single pulse)	0.5 A types	I_{Opk-}[2]	–	0.71	–	A	R_L = 0 Ω, t_p <10 µs
	2.3 A types		–	tbd	–		
Bootstrap diode forward voltage between VCC and VB (for types with bootstrap diode only)		$V_{F,BSD}$	–	1.0	1.3	V	I_F = 0.3 mA
Bootstrap diode forward current between VCC and	0.5 A types	$I_{F,BSD}$	30	55	80	mA	$V_{CC} - V_B$ = 4 V

[1] Not subject of production test, verified by characterisation
[2] Not subject of production test, verified by characterisation

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
VB (for types with bootstrap diode only)	2.3 A types		45	82	120		
Bootstrap diode resistance (for types with bootstrap diode only)	0.5 A types	R_{BSD}	24	40	60	Ω	V_{F1} = 4 V, V_{F2} = 5 V
	2.3 A types		15	27	40		
EN-/FLT low on resistance of the pull down transistor		$R_{on,FLT}$	–	45	100		$V_{EN-/FLT}$ = 0.5 V

4.6 Dynamic parameters

V_{CC} = V_{BS} = 15 V, V_S = V_{GND} = V_{PGND}, C_L = 180 pF unless otherwise specified. (T_A=25°C)

Table 7 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay	IGBT types	t_{on}	300	400	600	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
	MOSFET types		230	300	450		
Turn-off propagation delay	IGBT types	t_{off}	290	380	580		
	MOSFET types		210	280	420		
Turn-on rise time	0.5 A types	t_r	–	48	80		$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF (0.5 A) or C_L = 4.9 nF (2.3 A)
	2.3 A types		–	48	–		
Turn-off fall time	0.5 A types	t_f	–	18	30		
	2.3 A types		–	18	–		
Shutdown propagation delay ENABLE		t_{EN}	–	500	800		V_{EN}=0.5 V, V_{LO} / V_{HO} = 20%
Input filter time at LIN/HIN for turn on and off	IGBT types	t_{FILIN}	120	200	–		$V_{LIN/HIN}$ = 0 & 3.3 V
	MOSFET types HIN LIN		 50 tbd	 110 150	 150 tbd		
Input filter time EN		t_{FILEN}	100	300	–		
ITRIP filter time		$t_{FILITRIP}$	1.3	2.0	2.7	µs	V_{PGND} = 1 V, /FLT=0
Shut down propoagation delay PGND to any output		t_{ITRIP}	1.5	2.2	3.0		V_{PGND} = 1 V V_{LO} / V_{HO} = 3V
Propagation delay ITRIP to FAULT		t_{FLT}	1.4	2.1	2.8		V_{PGND} = 1 V, /FLT=0.5 V
Fault-clear time		t_{FLTCLR}	70	100	–		V_{PGND} = 0.1 V, /FLT=2.1 V
Dead time (not for 2EDL04I06BF)	IGBT types	DT	tbd	400	tbd	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
	MOSFET types		tbd	75	tbd		
Dead time matching abs(DT_LH – DT_HL) for single IC (not for 2EDL04I06BF)		MDT	–	20	tbd		ext. dead time 0ns
Matching delay ON, abs(ton_HS - ton_LS)		MT_{ON}	–	tbd	60		external dead time > 500 ns
Matching delay OFF, abs(toff_HS-toff_LS)		MT_{OFF}	–	tbd	60		external dead time >500 ns
Output pulse width matching. PW_{in}-PW_{out}	IGBT types	PM	–	20	80		PW_{in} > 1 µs
	MOSFET types		–	20	70		

5 Timing diagrams

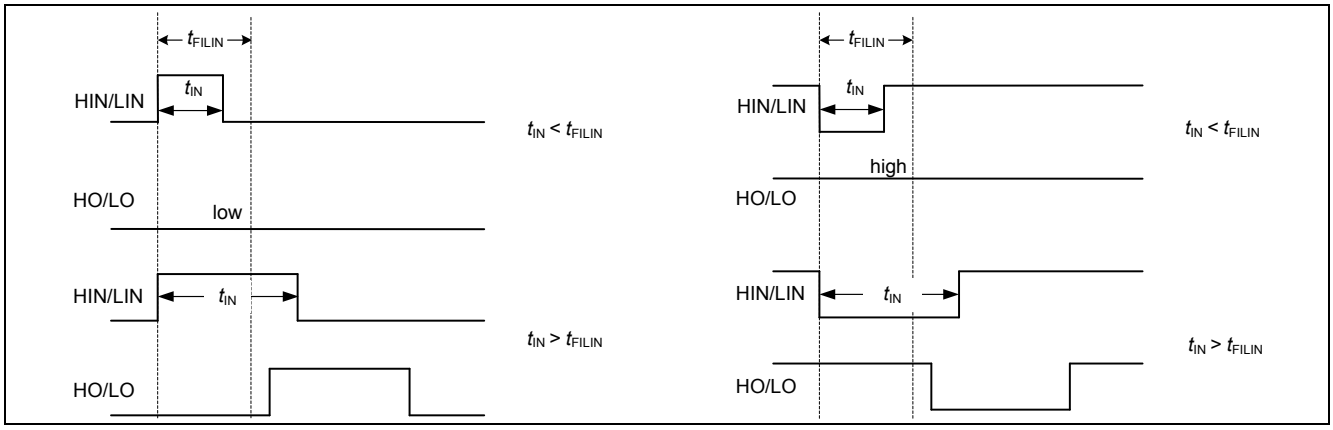

Figure 7 Timing of short pulse suppression

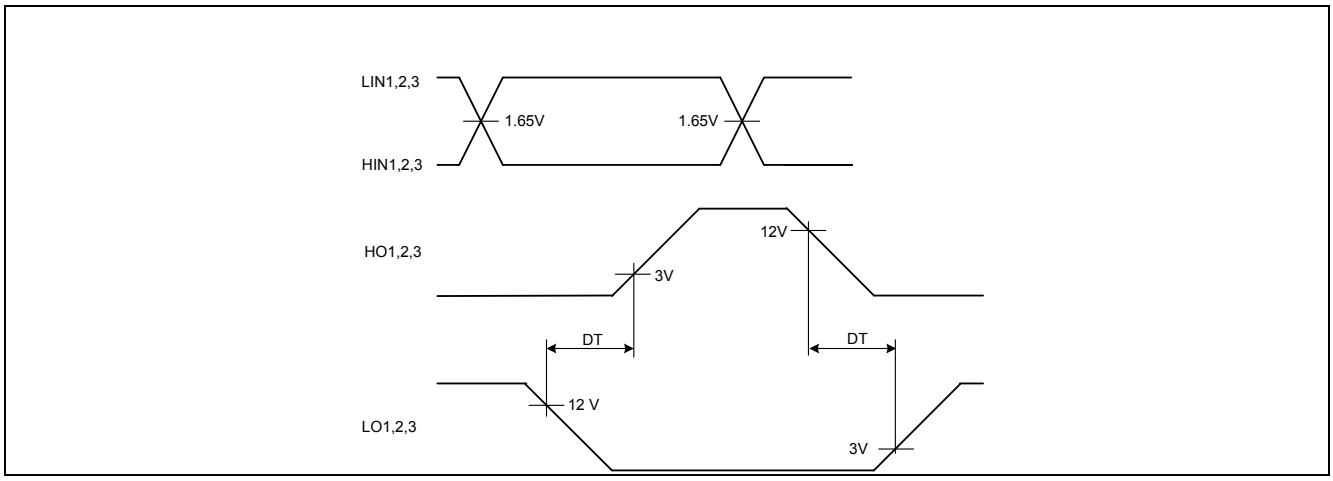

Figure 8 Timing of of internal deadtime

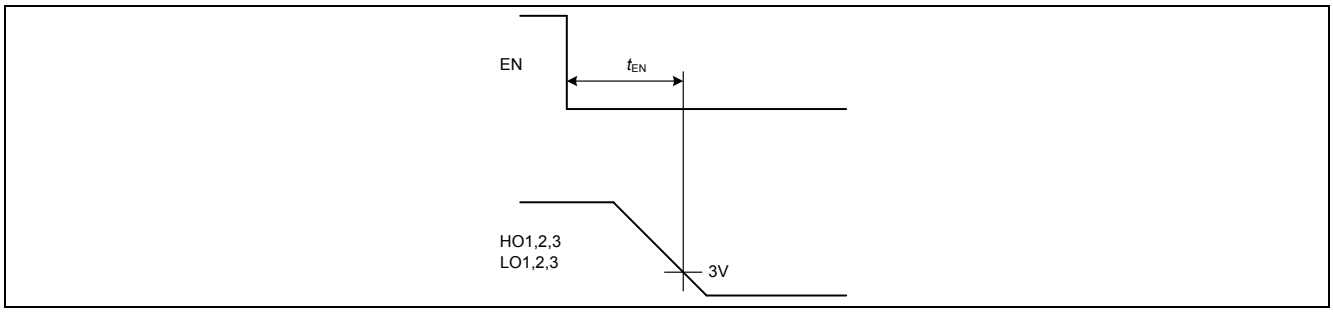

Figure 9 Enable delay time definition

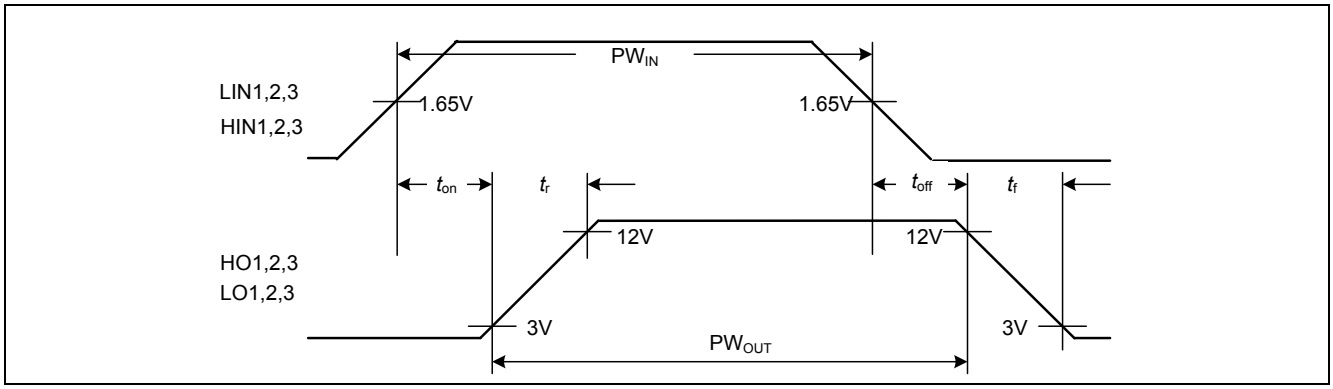

Figure 10 Input to output propagation delay times and switching times definition

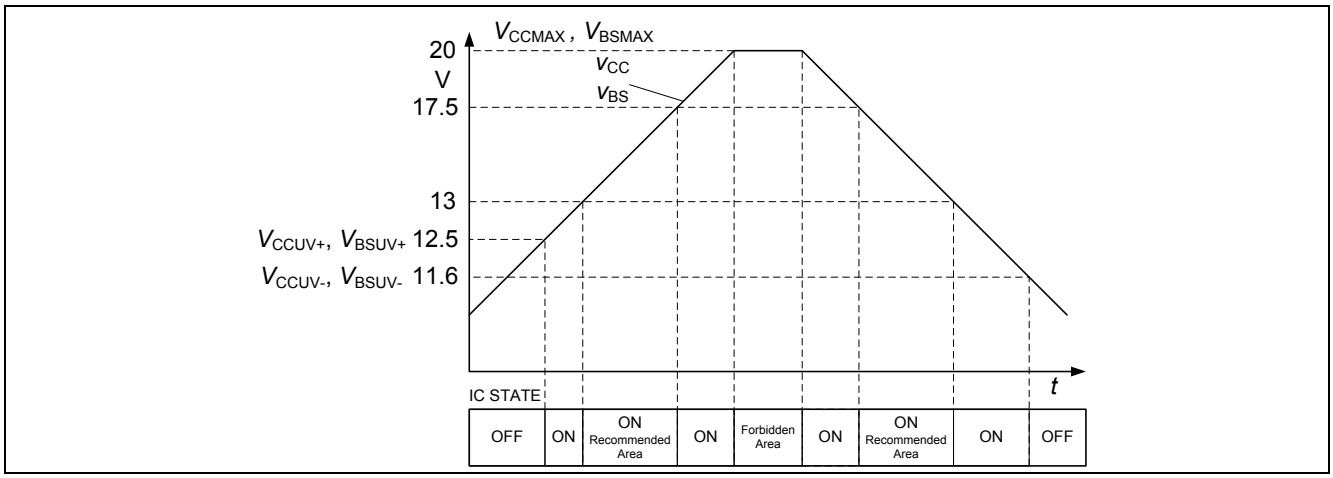

Figure 11 Operating areas (IGBT UVLO levels)

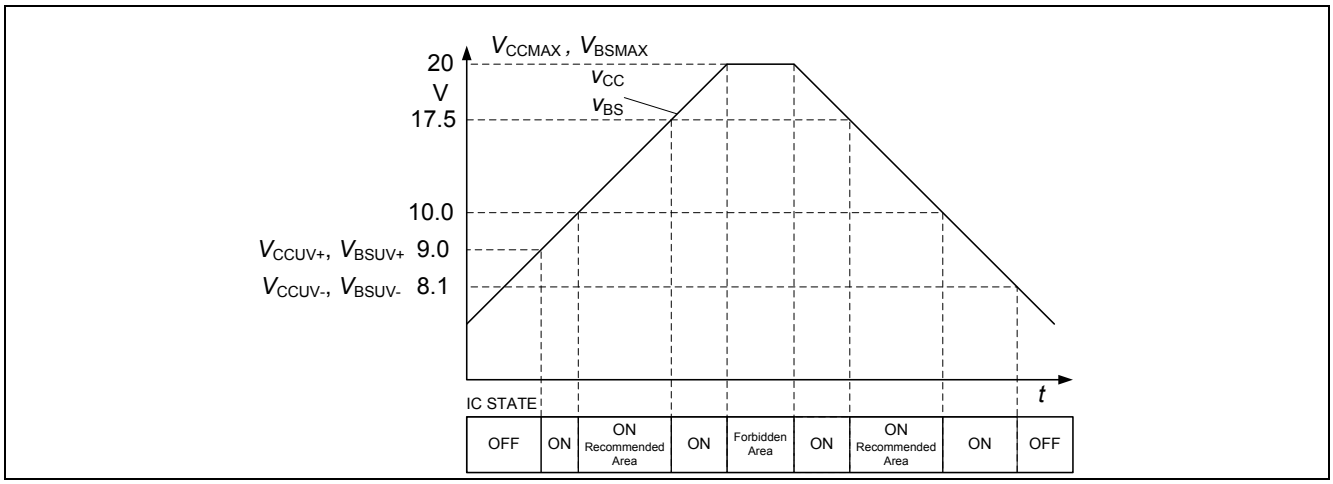

Figure 12 Operating areas (MOSFET UVLO levels)

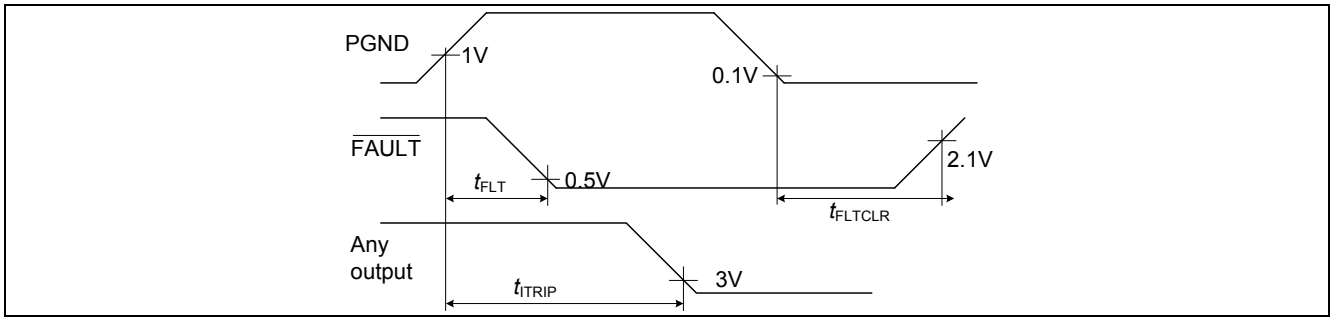

Figure 13 ITRIP-Timing

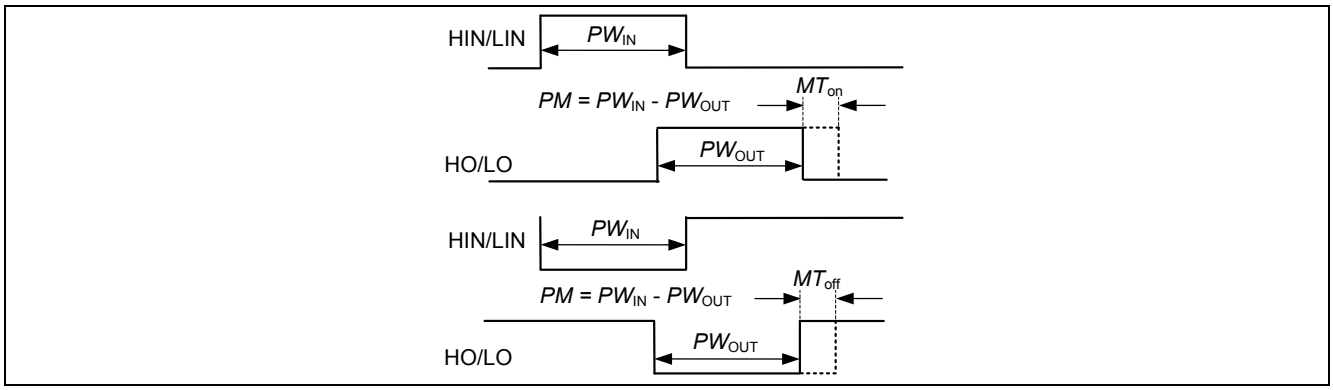

Figure 14 Output pulse width timing and matching delay timing diagram for positive logic

6 Package

6.1 PG-DSO-8

tbd

Max. reflow solder temperature: 265°C acc. JEDEC
Max. wave solder temperature: 245°C acc. JEDEC

Figure 15 Package drawing

Dimensions	80.0 × 80.0 × 1.5 mm³	λ_{therm} [W/m·K]
Material	FR4	0.3
Metal (Copper)	70µm	388

Figure 16 PCB reference layout

6.2 PG-DSO-14

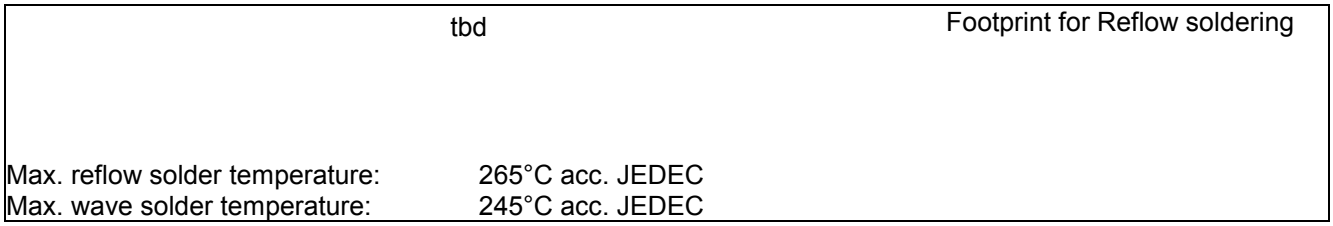

Figure 17 Package drawing

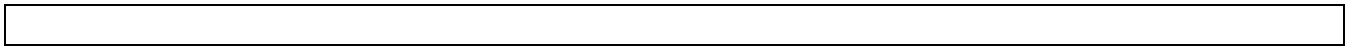

Figure 18 PCB reference layout (according to JEDEC 1s0P)
left: Reference layout
right: detail of footprint

Table 8 Data of reference layout

Dimensions	Material	Metal (Copper)
76.2 × 114.3 × 1.5 mm³	FR4 (λ_{therm} = 0.3 W/mK)	70µm (λ_{therm} = 388 W/mK)

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